Permanent Fault Repair in FPGAs through Graceful Degradation

Introduction

- Permanent fault recovery
  - Removing damaged elements
  - Repairing damaged elements

Permanent Fault Repair

- Module repair
  - Hybrid redundancy
  - Self-purging redundancy
    - TMR/Simplex
- Fine-grained repair
  - FPGA
    - Reconfiguration
    - Replacing damaged elements by unused fault-free elements

Error Recovery Flow in FPGAs

Permanent Fault Repair in FPGAs

- Problem addressed
  - Exhaustion of fault-free elements
    - High FPGA utilization
    - Long mission time

Catherine Shu-Yi Yu
Stanford University
April 16, 2001
Permanent Fault Repair in FPGAs through Graceful Degradation

Permanent Fault Repair in FPGAs
- Solution
  - Module removal
  - Availability degradation
  - Waste of resource

Configuration Selection
- Given
  - Original simplex design
  - Available FPGA area
- Find
  - Configuration
    - Availability

Design Candidates
- Starting from TMR
  - Hybrid TMR-Simplex-CED
  - Duplex with two CEDs
  - Duplex with a checker
- Designs adjusted with available FPGA area
  - Graceful degradation
    - Availability

Hybrid TMR-Simplex-CED
- Original
- Degraded
Permanent Fault Repair in FPGAs through Graceful Degradation

Hybrid TMR-Simplex-CED
- Partition of TMR and Simplex-CED
  - Available FPGA area
  - Design constraints
- Recovery
  - TMR
    - Roll-forward
  - Simplex-CED
    - Rollback

Duplex with Two CEDs
- Proportion with CED
  - Available FPGA area
  - Design constraints
- Recovery
  - Mismatch
    - Detection in one CED
    - Roll-forward
  - Detection in none or both CED
    - Rollback

Duplex with a Checker
- Checker area
  - Available FPGA area
  - Design constraints
- Recovery
  - Mismatch
    - Different with the checker
    - Roll-forward
  - Same with the checker
    - Rollback

Evaluation Metrics
- Rollback rate
  - Percentage of time in re-computation
  - Indication of availability
  - Important for deadline-critical applications
  - Calculation
    - \( \text{Prob(rollback)} \)
Evaluation Metrics

- Data Integrity
  - Correct outputs or error indication
    - Normal function
    - Recovery
    - Repair
  - Calculation
    - Plot vs. time

Evaluation Metrics Computation

- CED
  - Coverage
    - Duplex: single block fault detection
    - General CED: single fault detection
  - Overhead
    - Duplex: 100%
    - General: 90% [Mitra 00]
    - Arithmetic: 30% [Sparenmann 96]

Evaluation Metrics Computation

- Permanent error rate
  - < Transient error rate [Ohlsson 98]
  - > Multiple transient error rate
  - ≤ Multiple transient error rate
  - Need other techniques
- Compared to module removal
  - TMR => Duplex

Rollback Rate

- CED duplex

Rollback Rate

- CED 90% overhead
Rollback Rate
- CED 30% overhead

Data Integrity
- CED duplex, total area = 2.75×module area

Data Integrity
- CED 90%, total area = 2.75×module area

Data Integrity
- CED duplex, total area = 2.25×module area

Data Integrity
- CED 90%, total area = 2.25×module area

Improvement
- Depending on CED overhead
  - High overhead
    - Hybrid TMR-Simplex-CED
  - Low overhead
    - 3×module area Duplex with two CEDs
    - < 3×module area: hybrid TMR-Simplex-CED
Permanent Fault Repair in FPGAs through Graceful Degradation

Data Integrity

- CED 30%, total area = 2.75xmodule area

![Graph showing data integrity over time for different redundancy schemes.

Conclusion

- Flexibility of FPGA
  - Permanent error repair
  - Graceful degradation
    - Rollback rate
      - Compared with module removal
      - Improved

- Configuration selection
  - High CED overhead
    - Real-time: hybrid TMR-Simplex-CED
    - Non-real-time: 3 x module area: TMR => Duplex
  - Low CED overhead
    - 3 x module area Duplex with two CEDs
    - < 3 x module area: hybrid TMR-Simplex-CED
Permanent Fault Repair in FPGAs through Graceful Degradation

References