Partial Reconfiguration of FPGA

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Outline
- Overview of FPGA Architecture
- Reconfiguration Issues
- Partial Reconfiguration Algorithms
- Summery
- Reference

FPGA Architecture
- Configurable Logic Blocks (CLB)
  - Look-Up Table (LUT)
  - MUX
  - D Flip-Flop
- Interconnection
  - Connection Box (CB)
  - Switch Box (SB)
- I/O Block (IOB)

Reconfiguration Issues
- Performance aspect
  - Dynamic run-time reconfiguration
- Fault tolerance aspect
  - Affinity matching method [Mathur et. al. 95]
  - Node-covering method [Hanchek and Dutt 96]
  - Partial reconfiguration and incremental routing [Bhatia 98]

Partial Reconfiguration
- Problem Formulation
- Assumptions
  - Fault diagnosis available
  - CLB fault only
  - Sufficient empty CLB for reconfiguration
- Algorithms
  - Minimax Grid Matching
  - Move-by-shifting Strategy
  - Incremental Routing
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Minimax Grid Matching
- Bipartite matching problem
- Minimize the max. distance of the matched pair
- Upper bound for the matching length $O(\log^{1/4}N)$ in random distribution [Leighton and Shor 86]
- Iterative greedy algorithm
  - Initially set $L=1$
  - Adding matched pairs if distance < $L$ available
  - If not, increment $L$ and restart again
  - Worst-case $L$ needs $O(N^{1/2})$ iterations

Functionality Transplantation
- Problems with direct swapping

Incremental Routing
- Rip up logic block nets and interconnect nets
- Trace the original netlist to find the endpoints

Functionality Transplantation
- Move-by-shifting strategy

Incremental Routing
- Locally reroute the ripped nets to the new CLBs
- Set a small window size for routing
- Increment the window if no routing resource available at each iteration
- Select the optimal rerouting path
  - Cost function: $c(s) = \alpha \cdot BB(s) + \beta \cdot CGC(s) + \gamma \cdot SU(s) + \delta \cdot PC(s)$
  - $BB$: bounding-box function
  - $CGC$: channel group capacity
  - $SU$: segment utilization
  - $PC$: pin capacity
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Issues and Potential Solutions

- **Complexity**
  - Max. $O(N^{1/2})$ rounds for minimax grid matching
  - Max. $O(F_{c} F_{s}^{2W_{s}})$ for each incremental routing
- **Spare CLBs during initial compilation**
- **Routability**
  - Xilinx Virtex: direct paths between adjacent CLBs, buffered lines to SBs 6-block away
- **Pre-Compilation approach**

Summary

- **Partial Reconfiguration**
  - Minimax Grid Matching
  - Move-by-shifting Strategy
  - Incremental Routing
  - Pre-Compilation Approach

Reference