The Flat Earth & Single-stuck Fault Theories
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The Murphy Experiment
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The Murphy Experiment
- Sponsors
  - Hughes Aircraft and LSI Logic
- Collaborators
  - Advantest, DTS, Pycon and Credence

Objectives
- Evaluate Production Test Techniques
  - Identify Techniques
    - Minimum Test Cost
    - Maximum Product Quality and Reliability
  - Compare
    - Fault Models and
    - Production Defects

The Murphy Chip
- LSI Logic 150k CMOS Gate Array
  - (with Crosscheck™ embedded array)
- 25,000 Gate Design
- 120 pin Ceramic PGA Package
- 96 Signal Pins
- L eff = 0.7 mm
- 5 volt nominal supply voltage

The Murphy Chip
- Special Purpose Chip Design
  - Support (DFT) Circuitry
  - 5 different Combinational circuit designs
    - (Circuits Under Test or CUTs)
    - 3 control logic designs
    - 2 data path designs
    - 4 copies of each CUT
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Wafer Sort

- 30 test sets applied
- 5,491 dies evaluated
- 309 dies packaged

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Package Die Selection

- 116 Dies with “functional” Failures
- 20 Dies with VLV Failures Only
- 1 Die with Only IDDQ Failure
- 166 Good Dies
  - 309 ICs Overall

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Package Test

- Tester
  - Advantest T6671E VLSI Test System
  - 125MHz clock rate
- Test Time: 10 minutes per die on average
  - 5 minutes per good die
  - 20 minutes per interesting die
  - 10 minutes average

- Total Number of Test Patterns Applied
  - 1.4 Million plus $2^{24}$ Exhaustive Patterns
- Test conditions
  - 3 Supply Voltages
    - 1.7V, 2.5V, 5V
  - 4 Test Speeds
    - “rated” from Shmoo plot
    - 2/3 rated
    - Less than 1/3 rated
    - Faster than rated — 15% or 5% faster

- 265 test sets applied
  - 162 single stuck fault based
  - 60 delay fault
  - 10 weighted random
  - 2 verification vectors
  - 30 IDDQ
  - 1 exhaustive

- All 30 Test Sets Used in the Wafer Probe
- More Multiple-detect SSF Test Sets
  - 1, 2, 3, 4, 5, 7, 10, 12, 15-detect
- Test Sets Modified from Original Test Sets
  - Preceded by all-zero, all-one, bitwise complemented vectors
  - Reverse sequence
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Package Test

• IDDQ Measurements
  ◆ Wait time: 1ms
  ◆ Adaptive Resolution: 2nA — 200nA
  ◆ Measured at 5.25V, 2.5V, and 1.7V
  ◆ 6 different test sets
    ■ 5 based on pseudo-stuck model
    ■ 1 pseudo-random

Reminder

• Very Thorough Manufacturing Test
• Defects
  ◆ Normal Production Defects
  ◆ No artificially inserted defects

Testing Issues

• Boolean Test Effectiveness
  ◆ aka functional test, scan test, stuck-fault test
• Timing Tests
  ◆ At-speed (functional) or Transition (2 pattern)
• Reliability Tests
  ◆ IDDQ, VLV, SHOVE, Burn in
• Disclaimer
  ◆ Murphy chip results only

Stuck-fault Test Questions

Are stuck-fault tests effective?
Is 100% single-stuck coverage enough?
What’s better?
Is the stuck-fault model accurate?
Does the test vector order matter?

Production Test Questions

Are there timing defects?
What’s the best test for timing defects?
Can burn-in be avoided?
How many IDDQ vectors are enough?
How good are IDDQ test pattern sets?
How about VLV?
  ◆ Very Low Voltage
How about SHOVE?
  ◆ SHOrt Voltage Elevation
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**Conclusions**
- The conventional wisdom
- Is often wrong

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Future Research

- Alternatives to AT-SPEED testing
- Alternatives to Burn In
- New IDD Techniques
- Very Low Voltage Techniques
- New approaches to SHOVE testing
- BIST Techniques
- Fault models & fault grading capability

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CRC Research Activities

**TOPS Project** - completed
- Totally-optimized Synthesis
- High-level Synthesis System Using VHDL
- Optimizes Design for Specified Test Features
- BIST, Scan
- Inserts Embedded Checkers for Concurrent Test
- Share Functional and Test or Checker logic

**ROAR Project**
- Reliability Obtained by Adaptive Reconfiguration
- Use FPGAs for fault-tolerant reconfiguration

**ARGOS Project**
- Use ARGOS satellite to collect error data
- Compare Rad Hard and COTS boards
- Software Implemented Fault Tolerance Techniques

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CRC Research Activities

**ELF Project**
1. Elusive Failures
2. Early-life Failures
- Theoretical Research
- VLV Test - Very-Low-Voltage Test
- SHOVE Test - SHOrt Voltage Elevation Test
- Experimental Research - Compare Test Techniques
  - Murphy Test Chip Experiment
  - LSI Logic 0.7µm Gate Array Chip, Combinational Circuits
  - ELF 1 Test Chip Experiment
  - LSI G10-P 0.35µm Cell-based Chip
  - Combinational, 2901 processors
  - ELF 2 Test Chip Experiment
  - LSI G10-P 0.35µm Cell-based Chip
  - Mixed-signal DAC Cores

Support: DARPA, NSF, LSI, IBM, HP, CIS
Cooperation: ADVANCE, AMBIT, INTEL, PYCON

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