Low Power Fault Tolerance

Outline

- Introduction
- Motivations
- Problems
- Current Solutions
- Summary

Introduction

- Fault Tolerance
  - Correct execution in presence of fault
- Fault Avoidance
- Error Detection
- Error Recovery
  - Reconfigure
- Need for Redundancy
  - More power consumption

Questions

- What Type of Fault?
  - Transient
    - Re-execution
  - Permanent
    - Structural (physical) redundancy
- Required
  - Recovery time
  - Reliability
- Power Budget

Motivations

- Space Applications
  - NASA Remote Exploration and Experimentation (REE) project [1]
  - Cheaper spacecrafts
  - Smaller, lower power budget
  - Commercial electronic components
  - Autonomous navigation and on-board data processing
- Commercial Satellites
- Ubiquitous Portable Computing

Example 1: Mars Pathfinder

- Commercial VME Bus (no redundancy)
- Lander:
  - Flight computer: rad-hard RISC 6000
  - COTS DRAM (3D stack), Actel FPGAs, COTS EEPROM, VxWorks
- Rover: [2]
  - 80C85
  - Very limited power budget
Low Power Fault Tolerance

Example 2: Cassini Spacecraft
- 10.7 year Mission to Saturn [3], [4]
- Dual Redundant Architecture
  - Modules and bus
  - 1750A microprocessor
- Contact Once per Week
- Autonomous Fault Tolerance
  - Fail safe
  - Fail operational
  - Time-critical activities
  - Checkpoints

Problems (1)
- Low-Voltage Technologies [5]
  - Reduced noise margin
  - Early total dose failure
  - Reduced radiation tolerance
  - Long-term reliability

Problems (2)
- Sub-micron Feature Sizes [6]
  - Reduce voltage to avoid hot carrier reliability issue
  - Comparable in size to the diameter of the ion track
  - Microdose (localized dose) damage
    - Microscopic ionization
    - Subthreshold leakage

Problems (3)
- Rad-Hardening of Commercial Lines Expensive
- COTS with FT for SEU
  - May not be effective for high total dose
- Rad-Hard Multiproject Wafers
- UTMC and AMI
  - 32KB rad-hard PROM (anti-fuse based)
  - 500Krad, 40ns, low power, $3300
  - "Commercial rad-hard" components

Power in CMOS
- Power: \( P = P_s + P_d + P_{sc} \)
- Dynamic Power: \( P_d = C V^2 f a \)
  - Lower:
    - \( C \): switching capacitive load
    - \( V \): supply voltage
    - \( f \): switching frequency
    - \( a \): activity
- Performance Hit
  - Use higher parallelism

Power Reduction
- Approaches
  - Processes and materials
  - Microelectronics packaging
  - Circuit design
  - Architecture design
- Other Driving Forces
  - Cost of packaging and cooling
  - Reliability aspects
Low Power Fault Tolerance

Processes and Materials
- Low-Threshold Material (SOI)
- Less Leakage Current
- Ultra Low Power Group at Stanford [7]
  - Tunable low threshold CMOS process
  - 125-500mV supply voltage

Microelectronics Packaging
- 3D MCM Stacks
- Higher Redundancy at Function Level
- No Moving of Data off and on the Chip
- Wafer Scale Integration [8]
  - Low power, high speed, small volume
  - Low yield: redundancy, reconfiguration

Circuit Approaches
- Static Circuits
- Operate at a Range of Frequencies
  - Programmable clock rate
- Optimum Transistor Sizing in Tree Checkers [9]
- Self-Checking Circuits [10]
- Adiabatic Switching
  - Charge storage/recovery circuits [11]
- Lower Internal Voltage

Architectural Approaches (1)
- Power-On/Clock Only Active Modules
  - StrongARM, ARM 810
- Stand-By, Sleep Mode
  - Ultra low-power 486SX/GX
  - Power management
- Cold Spare vs. Hot Standby
  - Powered down spares subject to less total ionizing dose degradation
- Fuse Blower Chip to Isolate Faulty Module [12]

Architectural Approaches (2)
- Several Smaller Processing Elements with Spares [13]
- Built-in-Self-Repair Techniques
  - Yield enhancement
- Residue Codes for Arithmetic Units
- Adaptability
  - Trade off performance for fault-tolerance
- Graceful Degradation

Configurable Spare Processors
- Configurable Data Path [14]
  - One can do the job of any failing data path
- Synthesis Tools
  - Bundles of compatible applications
  - Configurable spare for each bundle
  - Each application in k bundles
- Area 71% of Dedicated Spare
Low Power Fault Tolerance

FT State Machines
- Correct Single Flip-Flop Errors [15]
  - TMR
  - Duplex
  - Different ECC approaches
  - TMR only in Flip-Flops
- Best area and performance
- M-of-N Codes
- Minimize Switching [16]
  - Number of bits changed per cycle

Temporal Redundancy
- Error Detection
  - Multiple execution of instructions
  - High latency
  - Affine transformations
- Error Recovery
  - Process pairs
- Important Jobs Duplicated
- Hybrid of Structural and Temporal Redundancy

Summary
- Critical Tasks
  - Structural redundancy
- Benefits from Low Power Technology
- ECC and Spare Column for Memory
- Self-Checking Circuits
- Residue Code for Data Path
- Configurable Spares
- Power Management
- Software Error Detection

References (1)
- Shaw, D.C., G.M. Swift and A.H. Johnston

References (2)
[7] Ultra Low Power group at Stanford:
  - [http://www-star.stanford.edu/projects/upul/upul.html]

References (3)

References (4)

Philipp Shirvani - RATS Page 4 7/28/97