Interconnect testing of FPGA

Problem Statement
- Detecting all faults in FPGA interconnect resources
  - Wire segments
  - Programmable interconnect points
    - Switch matrices
    - IO Muxes
  - Application independent test

Outline
- Introduction
- Previous work
- Limitations
- Theoretical aspects
- Suggested Methods
- Future Work

Virtex FPGA Model

Switch Matrix

Sparse Pipulation
- PIP : Programmable Interconnect Point
- One or path of pass transistors
- No PIP between each possible pair of pins
- Each node connectable to all others
- Proper positioning of PIPs
  - Switch matrix as a connected graph
  - some pairs connected via multiple PIPs
- Different delays between different pairs
  - Fewer pass transistors
  - More density
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Interconnect
- Hierarchy of interconnects
  - Single (link each adjacent CLB)
  - Hex (every 3 and 6 CLB)
  - Long (every 6 and 12 CLB)
- Longer lines are not necessarily slower
  - Fatter
  - Buffered
- Hierarchy to support speed and density

Previous Work
- BIST-based methods
  - Comparison-based
  - Parity-based
  - Bus-Based Testing

BIST-based Methods
- Wire Under Test (WUT)
- Comparison-based techniques [Stroud98]
  - Same test to two groups of WUT
  - Compare the results

BIST-based Methods
- Parity-based techniques [Sun00]
  - TPG generates parity line for k WUTs
  - ORA computes parity for k lines and compares it to original parity line
- Transparency of logic cells
  - Implement identity function

Parity-based BIST

Bus-based Testing
- Configure all wiring segments as long buses [Renovell 00, 98, 97]
- Bus : Multiple concatenated wires
- At least 3 configurations
  - Orthogonal
  - Diagonal-1
  - Diagonal-2
- Use conventional bus testing approaches
Limitations of Previous Work

- Too simplistic model of switch matrix
  - Connectable pairs table is not regular
- Almost neglect the hierarchy of interconnect
- Real implementation issue
  - How to read in and out the WUTs?
- Limitations in number of IOs per boundary cell
- Buffering and clocking long WUTs
  - Lack of at-speed test
  - Disability to detect delay faults

Theoretical Aspects

- ON-set
  - Set of all used PIPs in the configuration
- OFF-set
  - Set of unused PIPs that are incident with some used PIP at least one end
  - Able to detect stuck-at-off faults of ON-set
  - Causes open fault at line passing through
  - Able to detect stuck-at-on faults of OFF-set
  - Unused lines are driven
  - Causes short between incident lines

Example

\[
\begin{align*}
\text{ON-set} & = \{(N2,S2),(N3,S1),(E1,S3), (E3,W3)\} \\
\text{OFF-set} & = \{(N2,E2),(N3,S3),(S2,W1), (N1,S1),(E2,W3),(N1,E3), (E1,W1)\}
\end{align*}
\]

Theoretical Aspects

- Full PIP coverage
  - Detects all stuck-on and stuck-off of all PIPs
  - Enough number of configuration such that
    - Each PIP appears in at least one ON-set
    - Each PIP appears in at least one OFF-set
  - Full PIP coverage ≠ full interconnect coverage
  - Some shorts may still remain uncovered
  - Need other configurations to cover

Complete Configuration

- Each pin of switch matrix is incident to one and only one active PIP
- All unused PIPs are in OFF-set
- Corresponds to perfect matching problem
  - Switch matrix as a graph
  - Full PIP coverage =
    - Complete configurations to visit all PIPs
  - Polynomial time optimized algorithm[West 96]
  - Minimum number of configurations

Practical Limitations

- Need to at-speed testing
- Number of flip-flops per CLB
  - 4 per each CLB in current FPGAs
  - Limits the width of WUT
- Number of IOs per IO blocks
  - The same as above
- Restricted routing from O-Mux to Switch matrix
  - O-Mux : MUX from LE output to switch matrix
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Methods
- Bus testing
  - Wires passing only through switch matrices
- Scan testing
  - Wires passing through switch matrices, IO muxes, and flip-flops

Bus Testing
- Long concatenation of wires passing through switch matrixes

Bus Testing
+ No need to pass through logic blocks
+ Wider WUTs
  - More PIP coverage per configuration
- Very large propagation delay
  - Unable to detect delay faults
- Bus width (k1) limited by number of IO per IO blocks

Scan Testing
- Wires passing through switch matrixes and flip flops

Scan Testing
+ At-speed testing
  - More compatible with real designs
- Narrower WUTs
  - Width limited by number of FFs per CLB
  - Far less than number of compatible PIPs per switch matrix
  - More configurations to cover all PIPs

Solution
- Shifted scan testing
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**Shifted Scan Testing**
- Two categories of configurations
  - Orthogonal for EW, NS PIPs
  - Diagonal for NE, NW, SE, SW PIPs
- At-speed testing
  - Able to detect delay faults
- More concurrent WUTs
  - Less configurations
- Able to detect shorts among different WUTs

**Future Work**
- Considering IO-Muxes
- Configuration generation
  - Algorithm for full PIP coverage
  - Reasonable number of configurations
- Test Vector generation

**References**


