Using Test Results from a Sample of Chips to Reorder and Truncate Patterns

Outline
- Introduction
  - Pattern Choice and Order Problem
- Previous Engineers’ Solutions
  - Few Patterns Detect Defective Chips
- Our Contribution: Quantification
  - Few Patterns Detect Defective Chips
  - Defect Level Impact of Truncation
- Conclusion

Integrated Circuit Testing

<table>
<thead>
<tr>
<th>Inputs</th>
<th>CUT Outputs</th>
<th>Expected Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
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<td>10</td>
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<tr>
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<td>01</td>
<td>11*</td>
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<tr>
<td>101</td>
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<tr>
<td>111</td>
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Choice of Patterns to Apply
- Test Patterns Data
  - Storage in Tester Memory
- Limited Tester Memory
  - [Benware 03] [Maxwell 02] [Madge 04]
- Limited Number of Patterns on Tester
- Choice of Which Patterns to Apply
  - Defect Level Impact?

Stop on First Fail

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Choice of Order of Patterns
- Stop Testing after First Failing Pattern
  - Test Time Savings
- Reordering
  - Change in Test Time [Madge 04]
- Choice of Order of Patterns
  - And Truncation
Solution: [Maly 86]

- **Know**
  - Probability of Occurrence of Each Defect
  - Which patterns detect each defect
- **Pattern Order Criteria:**
  - Probability of detecting a defect
- **Optimum Order**
  - Minimum Testing Time
  - Minimum DPM Increase if Truncation

Problems with [Maly 86]

- **Do not Know**
  - Probability of Occurrence of Each Defect
  - Which patterns detect each defect
- **Solutions:**
  - Use of Test Metrics for Reordering
    - [Chao 04] [Cho 06] [Lin 01] [Tian 05]
  - Use of Test Results for Truncation
    - [Madge 04] [Guo 06] [Maxwell 02] [Benware 03]

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- **Conclusion**

First Patterns Detect Most chips

- [Guo 06] [Nigh 00] [Madge 04]
  - Power Curve
  - First Patterns
  - Detection of Most of Defective Chips
  - Example: 10%-90%

Few Patterns Detect Chips

- [Madge 04]: Test of 25 Wafers
  - 4% of Patterns Detect Chips
- [Guo 06]: Test of 500,000 Chips
  - 30% of Patterns Detect Chips
- [Nigh 00]: Test of 20,000 Chips
  - 11% of Patterns Detect Chips
Pattern Choice and Ordering

- Solution to Pattern Choice and Ordering
  - First Patterns Detect Most Defective Chips
  - Few Patterns Detect Defective Chips
- Problem:
  - Patterns Detecting Defective Chips
  - Prediction Hard

Evidence

- Experiments in [Madge 04]
  - Set of Patterns detecting Defective Chips
  - Different at Every Experiment
- Conclusion in [Guo 06]
  - "No Test Metric can Predict which Patterns will detect defective chips"

[Madge 04]

- First Experiment:
  - 6,000 patterns
  - 25 Wafers of Chips
  - Only 4% of patterns detect defective chips
- Second Experiment:
  - Same 6,000 Patterns, next 25 Wafers
  - Different 4% of patterns detect defective chips

[Guo 06]

- 7,400 patterns Test Set
- 500,000 Chips Tested
- Test Metrics to Test Results Comparison
  - Only 30% of the patterns detect defective chips
  - Conclusion: "No Test Metric can predict which patterns detect defective chips"

Test Time Gain by Prediction

- [Madge 04]
  - If Patterns Ordered Perfectly
    - Reduce 2-40x Defective Chips Test Time

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Few Patterns Detect Chips

- Expected Number of Useful Patterns
  - Defect Coverage of Patterns 1 through k \( C_D(k) \)
  - Number of Patterns \( N \)
  - Number of Chips Tested \( M \)
  - Yield \( Y \)

\[
N - \sum_{k=1}^{N} (1 - C_D(k - 1) + C_D(k))^M (1 - Y) 
\]

Derivation

- Defective Chips Passing Patterns 1 to n
  \[ 1 - C_D(n - 1) \]
- Defective Chips Passing Patterns 1 to n
  \[ 1 - C_D(n) \]
- \( P(\text{1 Chip Not Detected by } n) = C_D(n - 1) + (1 - C_D(n)) \)
- \( P(\text{No Chip Detected by } n) = (C_D(n - 1) + (1 - C_D(n)))^{Y(n - 1)} \)

Experiment Results

- IBM Experiment
- 10,000 Patterns Test Set
  - 1,000,000 Chips Tested
    - 3,000 Useful Patterns
  - 20,000,000 Chips Tested
    - 5,000 Useful Patterns

IBM Experiment Example

- Defective Chips Detected vs Patterns Applied
- The First 1,000 Patterns (10%) Detect 40,000 Defective Chips (50%)
- The Remaining 9,000 Patterns have only 5,000 Chips Left to Detect
- Conclusion: Not Enough Defective Chips Tested for All the Patterns to Fail

Conclusion

- Not Test Enough Defective Chips
  - For all patterns to fail
  - To predict whether a pattern will fail
  - Truncation?

Defect Level Increase

- Truncate Test Set
  - Less Thorough Test Set
- What Defect Level increase?
  - [Williams 81] [McCluskey 88b]
  - Too Conservative Estimate?
    - Loss of few useful patterns
    - Not all defects will occur
Defect Level Increase Calculation

- Assumption: All Defects Occur
- Wadsack [Wadsack 78]
  - Defect Coverage = Fault Coverage
- Williams-Brown [Williams 81]
  - Defect = Independent and Equiprobable SSF
- JSSC [Agrawal 82], CAD [Das 90], SPR [Seth 89]
  - Dependent Defects, Clustering

Williams-Brown

- Williams-Brown [Williams 81]
  - Defect Level = f( Yield, Coverage )

\[
\text{Defect Level} = 1 - \text{Yield}^{(1 - \text{Coverage})}
\]

[McCluskey 88b]

Estimates Too Conservative?

- 10,000 patterns: 99.5% SSF Coverage
  - 1,000,000 Chips Tested, 50,000 Detected
  - 3,000 Useful Patterns
- Truncate: 3,000 Patterns: 97% Coverage
  - [McCluskey 88b]: 256 DPM to 1,500 DPM
  - Statistics: Loose 7,000 Patterns
  - Only 295 are useful
  - All Defects Occur? Conservative Estimate?

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- How Engineers Truncated Test Sets
- Test Results Useless for Reordering
- Defect Level Increase Calculation
  - Conclusion

Conclusion

- Statistics: Not Test Enough Defective Chips
  - For all patterns to fail
  - To predict whether a pattern will fail
- Defect Level Impact of Truncation
  - All Defects Occur? Conservative Estimate?
References


References