DETECTING DELAY FLAWS BY VERY-LOW-VOLTAGE TESTING

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ABSTRACT

The detectability of delay flaws can be improved by testing CMOS IC's with a very low supply voltage -- between 2 and 2.5 times the threshold voltage V_t of the transistors. A delay flaw is a defect that causes a local timing failure but the failure is not severe enough to cause malfunctioning. Delay flaws caused by degraded signals and gates with lower drive capability than expected are considered This paper investigates the voltage dependence of the effects of delay flaws and derives the test conditions for them.

1. INTRODUCTION

Hao and McCluskey first showed in [1] that very-low-voltage (VLV) testing can detect flaws in CMOS IC's. *VLV testing* is a test method that operates a circuit-under-test (CUT) at reduced voltage and speed to detect functional (Boolean), timing, or IDDQ failures. A *flaw* is an imperfection in an IC that causes early-life or intermittent failure. It does not make the flawed IC malfunction but degrades the performance, reduces the noise immunity, or increases the leakage current. Examples of flaws are resistive shorts and threshold voltage shifts [1]. We have shown in a previous paper that VLV testing is most effective in detecting flaws in CMOS IC's when the supply voltage is set between $2V_t$ and $2.5V_t$, where V_t is the threshold voltage of a MOS transistor [2]. The threshold voltages of an NMOS transistor V_{tn} and that of a PMOS transistor V_{tp} are the same for most optimized technologies [3] [4] [5]. However, V_t should be the smaller of V_{tn} and V_{tp} if the threshold voltages of NMOS and PMOS transistors are different. The discussion in [2] was based on gate oxide shorts and metal shorts. Moreover, most results were measured through DC tests.

Timing failures occur when the delay of the manufactured component is different from the designed delay [6]. This paper considers the effectiveness of VLV testing in detecting timing failures. A circuit has a *delay flaw* (*non-operational delay fault*) if there is a timing failure but the circuit continues to work at the designed speed [6] [7]. *Flaw coverage* of a delay flaw is the range of the attribute of a flaw that can be detected by a test, such as the range of the resistance of a short that can be detected by a test [2]. We will first discuss the failure modes that cause timing failures and then analyze how VLV testing can help detect these timing failures.

A *delay fault* (*operational delay fault*) is a timing failure that makes a circuit fail to work at the designed speed but to be functional at a slower speed [6] [7]. There are several definitions for delay faults. We used the definition described above in this paper. Most studies on testing timing failures concentrate on the detection of delay faults. However, some timing failures that are embedded in short paths may not cause delay faults at normal operating conditions. Although delay flaws do not make the circuits malfunction at the normal operating condition, they may cause problems if the supply voltage changes during operations due to IR drops or simultaneous switching noise [8]. Other delay flaws, such as threshold voltage shifts, indicate reliability problems of CUTs. Therefore, delay flaws can cause early-life and intermittent failures and need to be detected.

Table 1 lists the causes of timing failures and the possible testing techniques for detecting them. Although all these may be detected by delay fault testing, the success of detection depends on the significance of the excess delay in the defective circuit. VLV testing can enhance the significance of the excess delays for some of the listed causes and thus improve their detectability. We will discuss this table in depth in this paper.

Table 1 Causes for timing failures and possible testing techniques for detection

Causes at transistor level	Detected by		
Transmission gate opens	V*	D**	
Threshold voltage shifts	V	D	
Diminished-drive gates	V	D	
Gate oxide shorts	V	D	I***
Metal shorts	V	D	I
Defective interconnect buffers	V	D	I
High resistance interconnects, via defects		D	
Tunneling opens		D	

* VLV Testing, **Delay Fault Testing, ***IDDQ Testing

A *degraded signal* is a signal whose V_{IH} is lower than the supply voltage or whose V_{IL} is higher than the ground voltage level. A *slow-to-rise* (*slow-to-fall*) signal has a longer rise (fall) time than designed. The timing failure modes can be degraded signals, slow-to-rise signals, slow-to-fall signals, or increased propagation delays. A gate driven by a degraded signal will have an increased delay. Because most timing failures can be either directly or indirectly caused by degraded signals or gates with lower driving strengths, we will focus on the delay flaws caused by these two failure modes. We first investigated the voltage dependence of the propagation delay of a CMOS inverter. *Weakly-driven* (WD) *gates* have no internal defects but their inputs are driven by degraded signals. Theoretical analysis shows that the delay ratio between a WD gate with a degraded signal at its input and a fault-free gate increases significantly when the supply voltage is reduced to between $2V_t$ and $2.5V_t$. This conclusion is also valid for the case when the CUT has diminished driving capability. We verified this conclusion by investigating the delay flaws caused by transmission gate opens, threshold voltage shifts, and diminished-drive gates.

All simulations shown in this paper were based on MOSIS HP CMOS26B 0.8 µm technology and MOSIS HP CMOS14TB 0.6 µm technology. For the 0.8 µm technology, the normal operating voltage is 5V. For the 0.6 µm technology, the normal operating voltage is 3.3V. For submicron or deep-submicron technologies, the interconnect delay becomes more significant than it used to be [8]. Proper amount of interconnects were added in all simulations to avoid biasing the results. We used HSPICE to perform all simulations. For all simulations, the same transistor parameters were used for all supply voltages. Burd compared the simulated results based on the same technique with the measured results [9]. The errors of delay measurements at low voltage were less than 12%.

This paper is organized in the following way. Section 2 lists the causes of timing failures at the transistor level and discusses their failure modes. Section 3 shows the voltage dependence of the propagation delay of a CMOS gate and discusses how VLV testing can improve the detectability of delay flaws. Section 4 describes the effectiveness of VLV testing in detecting three types of delay flaws: transmission gate opens, threshold voltage shifts and diminished-drive gates. Section 5 concludes the paper.

2. CAUSES AND FAILURE MODES OF TIMING FAILURES

Table 1 lists the causes of timing failures. Transmission gate opens occur when one of the transistors in a CMOS transmission gate is malfunctioning and cannot pass any signals. The output of a transmission gate with a transmission gate open can have a degraded signal. The gate following this defective transmission gate is weakly driven and thus has an excess propagation delay. Hot carrier effects and process variations can result in threshold voltage shifts, which make transistors have smaller transconductance and lower driving strengths [10] [11]. The propagation delays of gates with threshold voltage shifts increase. Moreover, the outputs of these gates have slow-to-fall signals because the effects of threshold voltage shifts are more serious in NMOS transistors. Some CMOS gates with high driving strength are built by connecting two or more smaller gates in parallel. These gates will have lower driving strength if one or more of the parallelly connected gates are broken and cannot pass any signals. CMOS gates can also be weakened if the gate widths become smaller due to either spot defects or process imperfections. The output of the diminished-drive gate will have slow-to-rise or slow-to-fall signals. Also, the propagation delay of the defective gate increases. Spot defects can cause gate oxide shorts [12], unexpected conducting shorts, or narrowed interconnects. Gate oxide shorts and unexpected conducting shorts can cause degraded signals and increase leakage currents in CUTs.

For deep submicron technologies, the interconnect delay is no longer negligible. Buffers are sometimes added to reduce the long interconnect delay. If the buffers are defective, they may cause different failure modes depending on the type of defects. They may have internal resistive shorts, which can cause degraded signals, high leakage current, longer gate delays, or longer interconnect delays. If open faults occur in the buffers, signals may not be able to pass through the buffers and thus, cannot pass through the long interconnects either.

Via defects, stress voids, and electromigration can increase the resistance of an interconnect and thus cause longer RC delay along the interconnect [13]. The signal propagating in a higher-resistance interconnect may be slow-to-rise or slow-to-fall. Tunneling opens allow CUTs to be functional at low frequencies but fail at higher frequencies [14]. Table 2 summarizes the failure modes of timing failures described above.

Table 2 Summary of failure modes of timing failures

Causes	Failure Modes
Transmission gate opens	Degraded signals
Threshold voltage shifts	Increased gate delays Slow-to-fall signals
Diminished-drive gates	Increased gate delays Slow-to-rise signals Slow-to-fall signals
Gate oxide shorts	Degraded signals Increased leakage
Metal shorts	Degraded signals Increased leakage
Defective interconnect buffers	Degraded signals Increased gate delays Increased RC delays Increased leakage Opens
High resistance interconnects, via defects	Increased RC delays Slow-to-rise signals Slow-to-fall signals
Tunneling opens	CUT fails at high frequencies

In this paper, we will discuss how VLV testing can improve the detectability of timing failures that are caused by degraded signals and transistors with lower driving capabilities. Gate oxide shorts and metal shorts have been discussed in [2]. Defective buffers in long interconnects can have the same defects that occur in logic gates. Thus depending on the failure modes, VLV testing, IDDQ testing, and Delay Fault testing can be used to detect them. On the other hand, due to the phenomenon that RC delays do not scale when the supply voltage is reduced [15], VLV testing can hardly improve detecting high resistance interconnects. Instead, high resistance interconnects can be detected by delay fault testing at normal operating voltage.

Since CUTs with tunneling opens can only be functional at very low frequencies (close to DC) [14], they behave similarly to stuck-open faults. Thus, tunneling opens are gross delay faults and cannot cause delay flaws. We will focus on the first three items in Table 1 and 2 in this paper.

3. VOLTAGE DEPENDENCE OF CMOS PROPAGATION DELAY

In this section, we show that VLV testing is most effective in detecting delay flaws when the supply voltage is around the value where the propagation delay of a circuit starts to change significantly as the supply voltage is reduced. Although VLV testing can detect more flaws as the supply voltage is reduced, the test time becomes much longer and noise margin reduces seriously if the supply voltage is further reduced to a small voltage [2]. Also, fault-free circuits should be still functional at the selected voltage. Hence, the supply voltage for VLV testing should be determined so that the improvement of the flaw coverage is significant but the test time will not be unreasonably long and fault-free circuits can still be functional.

Because of the nonlinear behavior during a transition, it is difficult to find a closed-form analytic solution for the propagation delay of a CMOS gate. Several authors provided equations to estimate the propagation delay of a CMOS gate [16] [17]. Equation 1, however, is a first-order estimation of the relation between the propagation delay T_d and the supply voltage of an inverter. This equation was also used in [18]. We used Equation 1 instead of others because it can show the relationship between the propagation delay of a CMOS gate and the operating supply voltage more directly.

$$T_d = \frac{C_L \times V_{dd}}{\mu C_{ox}(W/L)(V_{dd} - V_t)^2} = K\frac{V_{dd}}{(V_{dd} - V_t)^2} \quad (1)$$

Figure 1 compares the propagation delays calculated from Equation 1 and the simulated results of a CMOS inverter based on the 0.8 μm technology. The propagation delay was measured during the falling transition at the output of the inverter. The supply voltage in Fig. 1 was scaled by the threshold voltage of an NMOS transistor. The normal operating voltage, 5V, is $7V_{tn}$ for this technology. Figure 1 suggests that Equation 1 is a good approximation of the propagation delay of a CMOS gate.

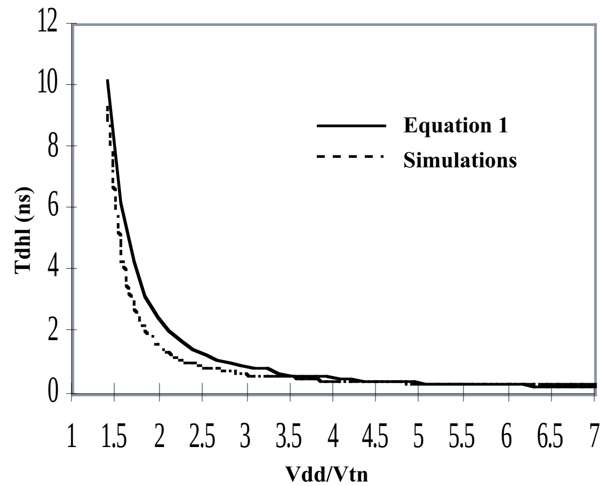

Figure 1 Comparison of gate delay values from simulation and from Equation 1

Figure 1 also shows that the propagation delay of a CMOS circuit increases monotonically as the supply voltage decreases from the normal operating voltage to V_t. It also implies that the increment of the propagation delay at low voltage is much more significant than that at the normal voltage.

If the input signal of a CMOS inverter is decreased from V_{dd} to V_{dd} / a, as shown in Fig. 2, the propagation delay T_{WD} of the WD inverter can be approximated by using Equation 2, in which a is a number greater than one, $T_d\ (V_{dd} / a)$ is the propagation delay of the inverter at V_{dd} / a, K is the same constant used in Equation 1.

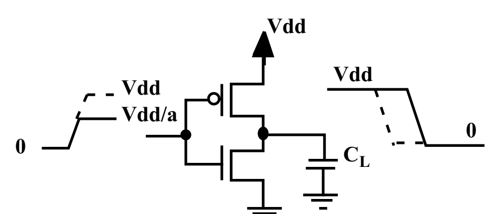

Figure 2 Effect of a degraded signal

$$T_{WD}(V_{dd}) = K\frac{V_{dd}}{(V_{dd}/a - V_t)^2} = aK\frac{V_{dd}/a}{(V_{dd}/a - V_t)^2} = a \times T_d(V_{dd}/a) \quad (2)$$

In Fig. 2, the solid lines represent the input and output signals of a WD gate and the dashed lines represent the same information for a fault-free gate. Based on Equation 2, the propagation delay of the WD gate can be approximated by the propagation delay of the inverter operating at V_{dd} / a multiplied by a. The *delay* *ratio* of a gate is the ratio between the delay of a faulty circuit and that of a fault-free circuit. The delay ratio of a WD gate is equivalent to the ratio between the delay of a fault-free circuit at V_{dd} / a and that of the same circuit at V_{dd} multiplied by a. In this case, the WD circuit is an inverter with a degraded signal at its input. Consequently, we can observe the voltage dependence of the propagation delay of a fault-free circuit to determine how the delay ratio of a CMOS gate changes at different voltages. This method can also be used for threshold voltage shifts. The derivation is straightforward . It can be found in the appendix of this paper. In this section, we focus on WD gates. The conclusion should also be valid for threshold voltage shifts. However, the voltage dependency of the delay ratio of a diminished-drive gate is more complicated. The slow-to-rise and slow-to-fall signals at the output of a diminished-drive gate complicate the delay prediction of the gate following the diminished-drive gate at different voltages. Thus, we will discuss the simulation results of diminished-drive gates directly in Sec. 4.

The *changing rate* of the propagation delay is the ratio of the propagation delays between two different voltages. If the propagation delay of a fault-free gate does not change much at some voltages, the delay ratio between a WD gate and a fault-free gate will be insignificant. On the other hand, if the supply voltage is in the range where the propagation delay of a fault-free gate changes significantly, the difference will be larger. In this paper, we use the changing rate of the propagation delay of a CMOS gate to quantify how significantly the propagation delay changes at each voltage. The supply voltage for VLV testing for detecting delay flaws should be set in the region where the changing rate of the propagation delay is significant. In this region, a small change in the supply voltage can cause a large change in the propagation delay. Thus, the difference between the propagation delay of a WD gate and that of a fault-free gate is much more significant.

Figure 3 shows the voltage dependence of the changing rate of the propagation delay of a CMOS gate. The changing rate of the propagation delay was measured as the ratio of the propagation delays between two voltages that differ by 0.2V. Similar to Fig. 1, the supply voltage is scaled by the threshold voltage of an NMOS transistor. Figure 3 shows that the changing rate of the propagation delay remains almost unchanged when the supply voltage is higher than $4V_t$. It starts increasing significantly when the supply voltage is reduced to about $2V_t$ to $2.5V_t$, which is the same as the voltage range for VLV testing suggested in [2].

Tables 3 and 4 list the delay ratios between WD and fault-free gates at different voltages for the 0.8 μm and 0.6 μm technologies. The input of the WD gate was degraded by 0.7V for the 0.8 μm technology and by 0.6V for the 0.6 μm technology. T_d (V_{dd}) was calculated by using Equation 1. T_{WD} (V_{dd}) was calculated by using

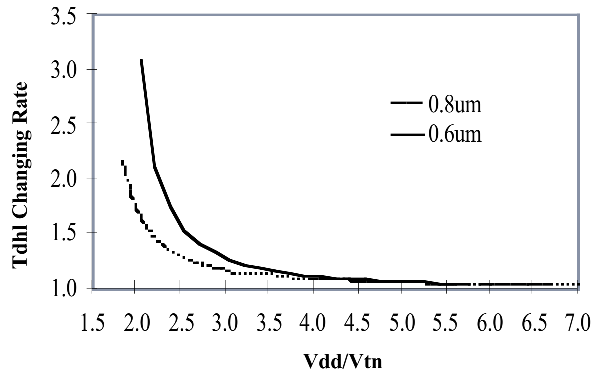

Figure 3 Voltage dependence of the changing rate of the propagation delay of a CMOS inverter

Equation 2. a is the ratio of a normal signal and a degraded signal. Based on the results, for both technologies, the delay ratios increase significantly when the supply voltage is in the range of $2V_t$ and $2.5V_t$. Sec. 4, we will use more complicated circuits to verify the conclusion based on the results in Tables 3 and 4.

Table 3 WD delay ratios for the 0.8 μm technology

V_{dd}	V_{dd} / V_{tn}	$T_d(V_{dd})^*$	a	$T_{WD}(V_{dd})^{**}$	Delay Ratio $T_{WD}(V_{dd})$/ $T_d(V_{dd})$
1.6	*2.24*	*1.70ns*	*1.78*	*33.71ns*	*22.8*
1.7	*2.38*	*1.46ns*	*1.70*	*17.37ns*	*11.9*
1.8	*2.52*	*1.27ns*	*1.64*	*10.09ns*	*7.9*
1.9	2.66	1.13ns	1.58	6.71ns	6.0
2	2.80	1.01ns	1.54	4.86ns	4.8
3	4.20	0.48ns	1.30	0.99ns	2.1
5	7.00	0.23ns	1.16	0.32ns	1.4

* based on Equation 1, ** based on Equation 2

Table 4 WD delay ratios for the 0.6μm technology

V_{dd}	V_{dd} / V_{tn}	$T_d(V_{dd})^*$	a	$T_{WD}(V_{dd})^{**}$	Delay Ratio $T_{WD}(V_{dd})$/ $T_d(V_{dd})$
1.3	*2.20*	*0.68ns*	*1.86*	*28.27ns*	*41.7*
1.4	*2.37*	*0.56ns*	*1.75*	*8.35ns*	*14.9*
1.5	*2.54*	*0.48ns*	*1.67*	*4.11ns*	*8.6*
1.6	2.71	0.41ns	1.61	2.50ns	6.1
2.0	3.39	0.26ns	1.43	0.80ns	3.0
3.3	5.59	0.12ns	1.22	0.20ns	1.7

* based on Equation 1, ** based on Equation 2

An analysis similar to Tables 3 and 4 was done for threshold voltage shifts. The threshold voltage of an NMOS transistor was increased by 0.3V for the 0.6 μm technology in this analysis. a (a_{sh} in Equation A2) increases from 1.1 to 1.33 and the delay ratio increases from 1.27 to 4 when the supply voltage is reduced from 3.3V to 1.2V (2.03 V_{tn}). Although the increments of the delay ratios for threshold voltage shifts are smaller than the numbers shown in Tables 3 and 4, CUTs may have global threshold voltage shifts. Thus, the path delay ratios can still be significant if CUTs have global threshold voltage shifts.

It is important to point out that the supply voltage for VLV testing should be set in the region where the changing rate of the propagation delay, instead of the propagation delay itself, starts to increase significantly. Although CMOS devices will have severe degradation in the speed performance if $V_{dd} < 4V_t$ [19], the changing rate of the propagation delay at $4V_t$ remains similar to that at the normal operating voltage. Moreover, if the supply voltage is set at the value where the changing rate of the propagation delay starts to increase significantly, we can keep the test time of VLV testing as short as possible and still improve the detectability of delay flaws.

4. DELAY FLAWS

In this section, we study three defects, transmission gate opens, threshold voltage shifts, diminished-drive gates, that can cause delay flaws in a CUT. Transmission gate opens can cause degraded signals in CUTs. In the previous section, we have shown that VLV testing is effective in detecting this type of delay flaw. Also, Hao and McCluskey have shown that VLV testing is effective in detecting threshold voltage shifts [1]. We will verify the supply voltage for VLV testing proposed in [2] is valid for detecting these timing failures too.

4.1 Transmission Gate Opens

4.1.1 Simulation Setup. We used part of a multiplier which consists of 4 levels of carry-save adders to simulate transmission gate opens. We picked this circuit because it is nontrivial and is not so large that it cannot be simulated in HSPICE. Figure 4 shows two pass-transistor logic implementations of a full adder cell. Figure 5 shows the interconnections of 12 full adder cells that form a 4-stage network. CSA11, CSA12, CSA13, CSA31, CSA32, and CSA33 use adder cell A. CSA01, CSA02, CSA03, CSA21, CSA22, and CSA23 use adder cell B.

There are five transmission gates in each full adder cell. Any transmission gate will have a degraded signal at its output if a transistor, either the NMOS or PMOS transistor, of the gate is stuck open. By stuck open, we mean one of the transistors in a CMOS transmission gate is malfunctioning and cannot pass any signals.

For this pass-transistor logic adder, the degraded signals that are caused by open faults in either T4 or T5 can rarely cause delay faults. This is because the outputs of T4 and T5 are connected to the gates of T1, T2, and T3. For example, if the PMOS transistor in T4 of an adder cell B is stuck open, the logic one at the output of T4 is degraded. This signal controls the NMOS transistor of T3. The inversion of the degraded signal, which has recovered to the normal voltage due to the inverter, controls the PMOS transistor of T3. Thus, T3 can still pass both high and low signals normally. By using the same argument, T1 and T2 can also pass signals normally. As a result, the degraded signal caused by the PMOS open fault in T4 has no direct effects on the outputs of the full adder cell. Similarly, the other open faults in T4 or T5 have no direct effect on the outputs of a full adder cell either. Also, due to the structure of the adder, a transistor open fault in T1 behaves similarly to a transistor open fault in T2. Consequently, we investigated the delay flaws caused by transistor open faults in T1 and T3.

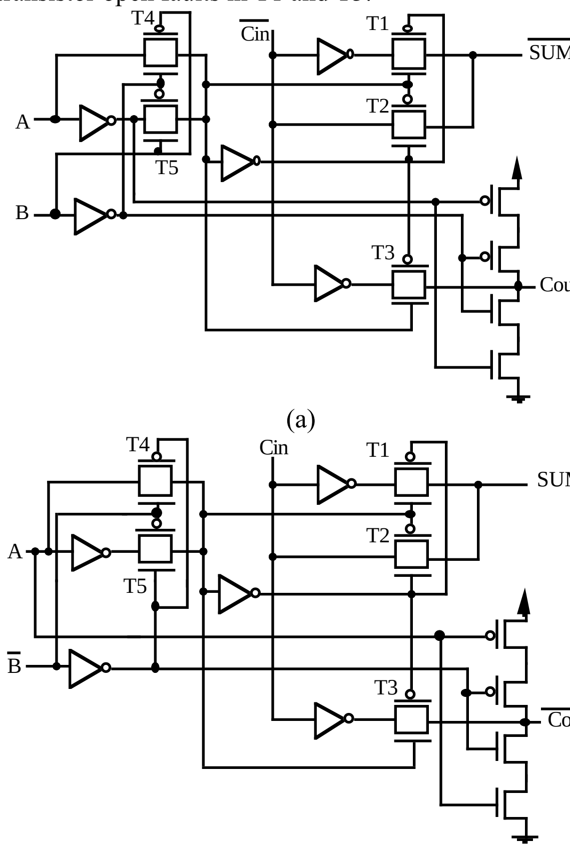

Figure 4 (a) adder cell A, (b) adder cell B

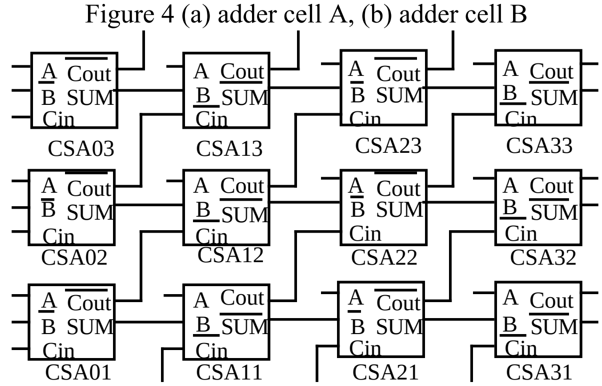

Figure 5 Simulation setup

Transmission gate opens were injected one at a time in T1 or T3 of the CSA11 and CSA22 cells in Fig. 5. The faults were injected into two different cells to show how the effectiveness of VLV testing changes due to different defect location. Table 5 lists the signal

Table 5 Signal propagating path

Defect Site		Signal Propagating Path
A	CSA11 T1 NMOS Open	CSA01(A)-CSA11(B)-CSA21(B)-CSA32(Cin)-CSA32(Cout)
B	CSA11 T1 PMOS Open	CSA01(A)-CSA11(B)-CSA21(B)-CSA32(Cin)-CSA32(Cout)
C	CSA11 T3 NMOS Open	CSA01(A)-CSA11(B)-CSA22(Cin)-CSA33(Cin)-CSA33(Cout)
D	CSA11 T3 PMOS Open	CSA01(A)-CSA11(B)-CSA22(Cin)-CSA33(Cin)-CSA33(Cout)
E	CSA22 T1 NMOS Open	CSA01(A)-CSA11(B)-CSA22(Cin)-CSA32(B)-CSA32(Cout)
F	CSA22 T1 PMOS Open	CSA01(A)-CSA11(B)-CSA22(Cin)-CSA32(B)-CSA32(Cout)
G	CSA22 T3 NMOS Open	CSA01(A)-CSA11(B)-CSA22(Cin)-CSA33(Cin)-CSA33(Cout)
H	CSA22 T3 PMOS Open	CSA01(A)-CSA11(B)-CSA22(Cin)-CSA33(Cin)-CSA33(Cout)

propagating path for each defect. The signal at node A of CSA01 was toggled in the appropriate direction to provoke the defect so that an excess delay can be observed at the selected output node of a WD CUT. All the inputs and outputs of the CUT were properly buffered by inverters.

4.1.2 Simulation Results. Tables 6, 7, 8, and 9 list the gate and path delay ratios between a faulty circuit, which has a transistor open fault in one of its transmission gates, and a fault-free circuit for both technologies used in this paper. The *gate delay ratio* is the ratio between the delay of a WD gate and that of a fault-free gate. The *path delay ratio* is the ratio between the delay of a path that is one of the paths shown in Table 5 and contains a WD gate and that of the same path with no WD gates. The interconnect delays were included in the measurements. In these tables, the rows that list the results of the supply voltage range for VLV testing concluded in Sec. 3 are italicized. Some of the entries in Tables 8 and 9 are "s-o", which stands for "stuck-open". The gate delay measured in these simulations is the delay of the CSA cell that follows immediately the cell with transmission gate open fault. This is because the faulty cell will cause signal degradation at its output once the defect is provoked, which will cause an excess propagation delay in the following cell. The path delay is measured from the input A of the CSA01 cell to the output Cout of the CSA32 or CSA33 cell.

For the 0.8 μm technology, the results in Tables 6 and 7 show that, if there is a PMOS open fault in T1 (T3) of the CSA22 cell, the gate delay ratio between WD and fault-free circuits is 1.1 (1.4) and the path delay ratio is only 1.1 (1.2) at the normal operating voltage, 5V. If these gates are not in the critical path of the CUT, the fault is unlikely to be detected at the normal operating voltage. However, the gate and path delay ratios increase significantly at low voltage. At 1.5V, which is $2.11V_{tn}$, the path delay ratio increases to 1.7 when T1 has a PMOS open fault and to 2.2 when T3 has a PMOS open fault. The driving strength of an NMOS transistor is larger than that of a PMOS transistor. Moreover, because $|V_{tp}|$ is larger than V_{tn} for this technology, the output signal of a CMOS transmission gate degrades more when there is an NMOS transistor open fault. Hence, the excess delay caused by an NMOS open fault in a transmission gate is much longer than that by a PMOS open fault. As a result, in a CMOS transmission gate, an NMOS open fault is more detectable than a PMOS open fault at any voltage. The results in Tables 6 and 7 also show that the enhancement of the effects of transmission gate opens at low voltage is similar when the defect is in either CSA11 or CSA22 cell. All the fault-free circuits were verified to be functional, although at very slow speeds, when the supply voltage was reduced as low as 1V for this technology. The results in Tables 6 and 7 verify the conclusions of Sec. 3. Based on the results, the effects of the delay flaws do not change very much when the supply voltage is reduced from the normal operating voltage to 2V ($2.81V_{tn}$). For example, when there is a PMOS open fault in T1 of the CSA22 cell, the path delay ratio only improves from 1.1 to 1.2 within this range. On the other hand, the path delay ratio improves more significantly when the supply voltage is further reduced to 1.5V ($2.11V_{tn}$).

Table 6 Gate delay ratios for the 0.8 μm technology

Supply Voltage			Gate Delay Ratio T_d (weakly-driven) / T_d (fault-free)							
V_{dd}	$\frac{V_{dd}}{V_{tn}}$	$\frac{V_{dd}}{V_{tp}}$	A	B	C	D	E	F	G	H
1.4	*1.97*	*1.56*	*42.2*	*3.7*	*57.7*	*9.0*	*33.6*	*3.6*	*60.5*	*8.8*
1.5	*2.11*	*1.67*	*37.1*	*3.4*	*56.4*	*7.5*	*30.7*	*3.2*	*60.8*	*7.5*
1.6	*2.25*	*1.78*	*30.2*	*3.0*	*49.3*	*6.3*	*25.3*	*2.8*	*52.8*	*6.2*
1.7	*2.39*	*1.89*	*22.7*	*2.6*	*39.7*	*5.3*	*19.6*	*2.2*	*42.2*	*4.9*
1.8	*2.53*	*2.00*	*18.1*	*2.3*	*32.8*	*4.5*	*15.9*	*2.0*	*35.4*	*4.0*
2.0	2.81	2.22	12.7	1.9	25.0	3.5	11.7	1.6	27.0	3.0
3.0	4.22	3.33	2.9	1.5	5.8	2.2	2.8	1.3	5.7	1.8
5.0	7.03	5.55	1.5	1.3	2.7	1.8	1.6	1.1	2.5	1.4

Table 7 Path delay ratios for the 0.8 μm technology

Supply Voltage			Path Delay Ratio T_d (faulty) / T_d (fault-free)							
V_{dd}	$\frac{V_{dd}}{V_{tn}}$	$\frac{V_{dd}}{V_{tp}}$	A	B	C	D	E	F	G	H
1.4	*1.97*	*1.56*	*10.7*	*2.0*	*16.5*	*3.0*	*12.3*	*1.9*	*15.1*	*2.5*
1.5	*2.11*	*1.67*	*9.9*	*1.8*	*15.9*	*2.7*	*11.2*	*1.7*	*14.8*	*2.2*
1.6	*2.25*	*1.78*	*8.4*	*1.7*	*13.6*	*2.4*	*9.6*	*1.6*	*13.1*	*2.0*
1.7	*2.39*	*1.89*	*6.6*	*1.5*	*10.8*	*2.1*	*7.6*	*1.4*	*10.7*	*1.7*
1.8	*2.53*	*2.00*	*5.5*	*1.4*	*9.0*	*1.9*	*6.1*	*1.3*	*8.9*	*1.6*
2.0	2.81	2.22	4.2	1.3	6.9	1.7	4.7	1.2	7.0	1.4
3.0	4.22	3.33	1.5	1.2	2.2	1.3	1.6	1.1	2.1	1.2
5.0	7.03	5.55	1.2	1.1	1.5	1.2	1.2	1.1	1.3	1.1

Turning to the 0.6 μm technology, the results in Tables 8 and 9 show that for all transmission gate opens in the CSA11 and CSA22 cells, the WD gates become stuck-open when the supply voltage is reduced to 1.2V, which is $2.03V_{tn}$. By stuck open here, we mean the WD gate does not switch when it is supposed to, no matter how long we wait. For each simulation, we waited for at least 500ns after the input switched before measuring the voltage at the output node. All the fault-free gates switched within 14ns when the supply voltage was between 1.2V and 3.3V for this technology.

Table 8 Gate delay ratios for the 0.6 μm technology

Supply Voltage			Gate Delay Ratio T_d (weakly-driven) / T_d (fault-free)							
V_{dd}	$\frac{V_{dd}}{V_{tn}}$	$\frac{V_{dd}}{V_{tp}}$	A	B	C	D	E	F	G	H
1.2	*2.03*	*1.43*	*s-o**	*s-o*	*s-o*	*s-o*	*s-o*	*s-o*	*s-o*	*s-o*
1.3	*2.20*	*1.55*	*s-o*	*49.8*	*s-o*	*165*	*s-o*	*54.2*	*s-o*	*167*
1.4	*2.37*	*1.67*	*s-o*	*13.9*	*s-o*	*42.3*	*s-o*	*14.8*	*s-o*	*43.5*
1.5	*2.54*	*1.79*	*s-o*	*6.5*	*s-o*	*18.5*	*s-o*	*6.9*	*s-o*	*17.5*
1.6	2.71	1.91	s-o	4.2	s-o	10.8	s-o	4.4	s-o	10.6
1.7	2.88	2.02	s-o	3.3	s-o	7.3	s-o	3.2	s-o	7.1
1.8	3.05	2.14	150	2.6	568	5.7	183	2.5	619	5.3
2.0	3.39	2.38	15.3	2.0	47.6	4.0	18.4	1.9	47.2	3.6
3.3	5.59	3.93	1.8	1.4	3.3	2.0	2.0	1.2	3.2	1.6

* stuck-open

Table 9 Path delay ratios for the 0.6 μm technology

Supply Voltage			Path Delay Ratio T_d (faulty) / T_d (fault-free)							
V_{dd}	$\frac{V_{dd}}{V_{tn}}$	$\frac{V_{dd}}{V_{tp}}$	A	B	C	D	E	F	G	H
1.2	*2.03*	*1.43*	*s-o**	*s-o*	*s-o*	*s-o*	*s-o*	*s-o*	*s-o*	*s-o*
1.3	*2.20*	*1.55*	*s-o*	*18.2*	*s-o*	*42.9*	*s-o*	*19.3*	*s-o*	*32.4*
1.4	*2.37*	*1.67*	*s-o*	*5.5*	*s-o*	*11.9*	*s-o*	*5.7*	*s-o*	*8.6*
1.5	*2.54*	*1.79*	*s-o*	*2.9*	*s-o*	*5.6*	*s-o*	*3.0*	*s-o*	*4.0*
1.6	2.71	1.91	s-o	2.1	s-o	3.6	s-o	2.1	s-o	2.6
1.7	2.88	2.02	s-o	1.8	s-o	2.7	s-o	1.7	s-o	2.1
1.8	3.05	2.14	44.8	1.5	112	2.2	53.0	1.5	142	1.7
2.0	3.39	2.38	5.3	1.4	10.7	1.8	6.1	1.3	11.4	1.4
3.3	5.59	3.93	1.3	1.1	1.6	1.3	1.3	1.1	1.5	1.1

* stuck-open

The reason for the occurrence of the stuck-open behavior in a WD circuit at low voltage is that the degraded signal is lower than the threshold voltage of a transistor. For example, at 1.2V, the degraded signal for logic one is 0.61V ($=V_{dd} - V_{tn}$) when there is a PMOS open in a transmission gate. The degraded signal is too low to turn on any NMOS transistors in the following gate. Similarly, the degraded signal for logic zero is 0.84V ($= |V_{tp}|$) when there is an NMOS open in a transmission gate. At 1.7V, the degraded signal cannot turn on any PMOS transistors in the following gate. For this technology, all fault-free circuits are functional when the supply voltage is between 0.9V and 3.3V.

The results of Tables 8 and 9 also show that the effects of the delay flaws are not very serious unless the supply voltage is low enough. The supply voltage for VLV testing should be as low as $2V_t$ to $2.5V_t$ to achieve reasonable improvement in the flaw coverage for delay flaws. If V_{tn} and $|V_{tp}|$ are different, V_t should be the smaller of them to ensure enough flaw coverage for flaws in both PMOS and NMOS transistors.

Although the defects presented in this section increase the quiescent current, the amount of increase depends on the sizes of the transistors that are connected to the outputs of a faulty transmission gate and the difference between the threshold voltages of an NMOS and a PMOS transistor. Therefore, these defects may not be detected by IDDQ testing.

4.2 Threshold Voltage Shifts

Threshold voltage shifts can be caused by process variations or hot carrier effects. Process variations can cause global threshold voltage shifts. On the other hand, hot electrons can cause global or local threshold voltage shifts. The discussions in this subsection concentrate on finding the appropriate supply voltage for VLV testing for detecting threshold voltage shifts.

If a transistor has a larger threshold voltage than expected, its transconductance is smaller. As a result, the transistor has lower driving capability and causes an excess delay during a transition. However, at the normal operating voltage the magnitude of the excess delay is insignificant if the threshold voltage is shifted by a small amount. By reducing the supply voltage, the degradation of the driving capability of a transistor becomes more significant and causes a longer delay. Additionally, threshold voltage shifts only degrade the speed performance of a CMOS gate. The static current of a faulty gate with threshold voltage shift does not increase.

A buffer chain with 6 inverters, as shown in Fig. 6, was simulated to characterize the behavior of a circuit with threshold voltage shift. Only the 0.8 μm technology was used for the simulations in this section. This is because we used BSIM1 (Berkeley Level 4; HSPICE Level 13) model for the HSPICE simulations of the 0.6μm technology. The threshold voltage of a transistor cannot be changed manually in this model. Both global and local threshold voltage shifts were investigated. VLV testing is more effective in detecting global threshold voltage shifts. Thus, we will investigate the supply voltage for VLV testing based on the simulation results of global threshold voltage shifts. We will then discuss the detectable range of local threshold voltage

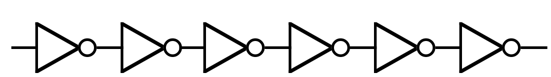

Figure 6 CMOS inverter chain

shifts at the proposed voltage.

Because the mobility of a hole is smaller than that of an electron, hot carrier effects are less significant for a PMOS transistor than an NMOS transistor. Consequently, threshold voltage shifts are smaller for PMOS transistors. As a result, we only investigated the effects of threshold voltage shifts at different voltages in NMOS transistors. For the simulations of global threshold voltage shifts, the threshold voltages of all the NMOS transistors were shifted by 0.2V, 0.3V, and 0.4V. For the simulations of local threshold voltage shifts, only the threshold voltage of the NMOS transistor in the second inverter in the chain was shifted. The amount of the threshold voltage shift in a damaged device could grow larger than the values simulated here if the gate leakage current caused by hot-electron injection stays longer [20]. Tables 10 and 11 show the simulation results. The last three columns in Tables 10 and 11 show the delay ratios. In this subsection, the *delay ratio* is the ratio between the propagation delay of a faulty circuit with threshold voltage shifts and that of a fault-free circuit. The delay measured in the simulations for global threshold voltage shifts is the propagation delay from the input of the second inverter to the output of the fifth inverter. In the same simulations, because the delay ratios of the rising and falling transitions are almost the same, only the delay ratio of the falling transition is shown in Table 10. For local threshold voltage shifts, the measured delay is the gate delay of the faulty circuit. Since only the rising transition at the input of the faulty gate can provoke the defect, the delay ratio of this transition is shown in Table 11.

Table 10 Delay ratio of a faulty circuit with global threshold voltage shifts vs. a fault-free circuit

Supply Voltage			Delay Ratio T_d (faulty) / T_d (fault-free)		
V_{dd}	V_{dd}/V_{tn}	V_{dd}/V_{tp}	$\Delta V_t = 0.2V$	$\Delta V_t = 0.3V$	$\Delta V_t = 0.4V$
1.3	1.83	1.44	1.34	1.67	2.37
1.4	1.97	1.56	1.28	1.53	1.98
1.5	2.11	1.67	1.25	1.43	1.74
1.6	2.25	1.78	1.21	1.40	1.61
1.7	2.39	1.89	1.20	1.32	1.56
1.8	2.53	2.00	1.19	1.31	1.46
1.9	2.67	2.11	1.19	1.23	1.43
2.0	2.81	2.22	1.13	1.24	1.36
5.0	7.03	5.55	1.06	1.08	1.09

For global threshold voltage shifts, we assume a defect is detectable if the delay of a faulty circuit increases by 25%. At the normal operating voltage, the delay ratio between a faulty circuit with a 0.2V global threshold voltage shift and a fault-free circuit is only 1.06, which is undetectable. Similar to the results shown in the previous subsection, the detectable range of global threshold voltage shifts does not change significantly from 5V to 2V. The supply voltage needs to be as low as 1.5V to catch a 0.2V global threshold voltage shift. This voltage value is $1.67|V_{tp}|$ or $2.11V_{tn}$. Therefore, a supply voltage of $2V_t$ to 2.5 V_t, as proposed in the [2], can offer reasonable flaw coverage for global threshold voltage shift, where V_t is the smaller of V_{tn} and $|V_{tp}|$.

For a local threshold voltage shift, the slack of the path and the magnitude of the increased gate delay determine whether the defect can be detected by a delay test. Table 11 shows that the ratio between the gate delay of a faulty gate with threshold voltage shift and that of a fault-free gate increases significantly at low voltage. Based on the results in Table 11, at the normal operating voltage the delay ratios are only around 1.1 when the threshold voltage is shifted by 0.2V or 0.3V, which is undetectable. At 1.5V, which is $2.11V_{tn}$ or $1.67|V_{tp}|$, the ratios increase to 1.72 when the threshold voltage is shifted by 0.3V. Although the detectability of local threshold voltage shifts depends on the slack of the path in which the faulty gate is embedded, the effects of the defects are more severe at low voltage.

Table 11 Delay ratio of a faulty circuit with local threshold voltage shifts vs. a fault-free circuit

Supply Voltage			Delay Ratio T_d (faulty) / T_d (fault-free)		
V_{dd}	V_{dd}/V_{tn}	V_{dd}/V_{tp}	$\Delta V_t = 0.2V$	$\Delta V_t = 0.3V$	$\Delta V_t = 0.4V$
1.3	1.83	1.44	1.54	2.01	2.98
1.4	1.97	1.56	1.47	1.85	2.47
1.5	2.11	1.67	1.41	1.72	2.18
1.6	2.25	1.78	1.36	1.63	2.04
1.7	2.39	1.89	1.36	1.57	1.82
1.8	2.53	2.00	1.34	1.44	1.73
1.9	2.67	2.11	1.30	1.41	1.63
2.0	2.81	2.22	1.26	1.42	1.63
5.0	7.03	5.55	1.11	1.18	1.25

4.3 Diminished-Drive Gates

In order to provide enough drive strength for either long interconnects or large loading, some gates are designed to be parallelly connected and thus avoid using large components devices. Figure 7 shows an example. One of the two inverters (in gray) in the high-drive gate malfunctions and cannot pass any signals. Three simulations were done. Each has a 100 μm, 500 μm, or 1000 μm long interconnect between the output of the high-drive gate and the 8 NAND gates. All input and output nodes were properly buffered. The propagation delay was measured from V_{A0} to V_{out1}, which are defined in Fig. 7. The interconnect delay is 38% of the measured delay at the normal operating voltage for the 100 μm case, 53% for the 500 μm case, and 58% for the 1000 μm case. The signal was set up so that there was a rising transition at the output of the faulty gate. Because NMOS transistors have stronger driving strength than the PMOS transistors, the faulty effect was more significant when the PMOS transistor in the faulty gate drove the output of the faulty gate. Also, because the simulation results for the 0.8 μm technology and 0.6 μm technology are similar, only the results for the 0.6 μm technology are discussed in this paper.

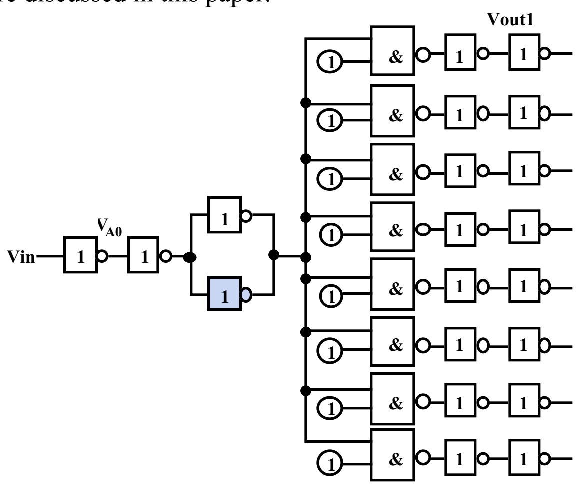

Figure 7 Diminished-drive gate

Table 12 shows the simulation results for the 0.6 μm technology. The delay ratio improves from 1.11 to 1.81 when the supply voltage is reduced from 3.3V ($5.59V_{tn}$) to 1.2V ($2.03V_{tn}$) when the wire length between the output of the high-drive gate and the inputs of the NAND gates is 1000 μm. The excess delay increases monotonically as the supply voltage is reduced.

Weak gates with smaller gate widths caused either by spot defects or process imperfections can also have diminished driving capability. The conclusion based on the simulations done in this subsection can also be generalized to the weak gates described above.

Table 12 Delay ratio between faulty and fault-free high-drive gate in Fig. 7 for the 0.6 μm technology

Supply Voltage			Delay Ratio T_d (faulty) / T_d (fault-free)		
V_{dd}	V_{dd} / V_{tn}	V_{dd} / V_{tp}	wire length =100 μm	wire length =500 μm	wire length =1000 μm
1.1	*1.86*	*1.31*	*3.23*	*2.84*	*2.30*
1.2	*2.03*	*1.43*	*3.07*	*2.43*	*1.81*
1.3	*2.20*	*1.55*	*2.93*	*2.11*	*1.56*
1.4	*2.37*	*1.67*	*2.74*	*1.85*	*1.39*
1.5	*2.54*	*1.79*	*2.66*	*1.68*	*1.30*
2.0	3.39	2.38	2.27	1.36	1.17
3.3	5.59	3.93	1.87	1.22	1.11

4.4 Supply Voltage for VLV Testing for Detecting Timing Failures

In summary, VLV testing can make delay flaws more detectable. It increases the significance of a gate delay fault and makes it more detectable even if the fault exists in a short path (non-critical path). Not only can VLV testing improve the detectability of the delay flaws discussed in this paper, but it should also be able to improve the detectability of other delay flaws that are caused by reduced signal levels.

Through extensive simulations, we justified that the supply voltage proposed in [2] for VLV testing is also valid when delay flaws are considered. The supply voltage for VLV testing should be in the range of $2V_t$ and $2.5V_t$, where V_t is the smaller of V_{tn} and $|V_{tp}|$. The delay flaws considered in this section are not guaranteed to be detected by current tests. Moreover, VLV testing works when the total leakage current is too big for IDDQ testing [2]. Low voltage technologies have lower threshold voltages to improve their performance [19]. Although a substrate back-biasing technique can be used to reduce the quiescent currents of these technologies [21], it adds complexity in the development of technologies and circuit operations and thus increases the cost.

4.5 Test Speed for VLV Testing for Detecting Timing Failures

To achieve good flaw coverage for delay flaws, the test speed for VLV testing must be determined accurately. We have presented two methods for determining the test speed for VLV testing in a previous work [2]. Because interconnect delay may become more significant for deep submicron technologies, the test speed selection should not ignore the existence of interconnect delay. Also, as IC's become denser and more complicated, it is more difficult to predict the test speed at different voltages theoretically or by simulations. Thus, more characterization of CUTs at low voltage, such as Shmoo plots, is necessary to determine the test speed of VLV testing to ensure the test quality.

5. CONCLUSIONS

Most timing failures are due to degraded signals or transistors with lower driving capabilities. We discussed how VLV testing can improve the detectability of the timing failures caused by degraded signals or gates with lower driving capabilities. The supply voltage for VLV testing for detecting delay flaws should be set in the region where the changing rate of the propagation delay of a CMOS gate starts increasing significantly. For both technologies used in this paper, the changing rate of the propagation delay of a CMOS inverter starts increasing when the supply voltage is between $2V_t$ and $2.5V_t$. We then simulated more complicated circuits to justify this statement. The flaws considered in this paper include transmission gate opens, threshold voltage shifts, and diminished-drive gates. The effects of delay flaws become significant when the supply voltage is set between $2V_t$ and $2.5V_t$. This conclusion is the same as that in a previous study [2].

The test speed for VLV testing needs to be selected carefully to ensure good test quality. For deep submicron technologies, interconnect delays may dominate and thus are no longer negligible. To find an accurate test speed, more characterization on CUTs is needed.

Delay flaws can cause early-life and intermittent failures and are hard to detect at normal operating conditions. VLV testing provides an effective and low-cost option to detect these marginal timing problems. It can be applied even when the leakage current of a CUT is too big for IDDQ testing. It can also help reduce the need to do burn-in.

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APPENDIX

Threshold Voltage Shifts

Equation A1 shows the propagation delay of an inverter with threshold voltage shifts. T_{sh} is the propagation delay of the faulty inverter with threshold voltage shifts. ΔV_t is the amount of threshold voltage shift. $T_d\ (V_{dd} - \Delta V_t)$ is the propagation delay of a fault-free inverter operating at $V_{dd} - \Delta V_t$. a_s of Equation A1 is shown in Equation A2. Hence, for threshold voltage shifts, we can also study the voltage dependence of the propagation delay of a fault-free gate to estimate the delay ratios between faulty and fault-free gates at different voltages.

$$\begin{aligned} T_{sh}(V_{dd}) &= K\frac{V_{dd}}{(V_{dd}-\Delta V_t - V_t)^2} \\ &= K\frac{V_{dd}}{(V_{dd}-\Delta V_t)}\times\frac{(V_{dd}-\Delta V_t)}{((V_{dd}-\Delta V_t)-V_t)^2} \\ &= a_s \times T_d(V_{dd}/a_s) \qquad \text{(A1)} \end{aligned}$$

$$a_s = \frac{V_{dd}}{(V_{dd}-\Delta V_t)} \qquad \text{(A2)}$$